What is claimed is:

1. A memory array, comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

a number of wordlines coupled to the gate region of at least one memory cell;

at least one strapping line of lower resistance than the wordlines coupled to at least one of the number of wordlines wherein the strapping line bypasses a portion of the wordline; and

at least two channels connecting the strapping line to the wordline.

2. The memory array of claim 1 wherein the strapping line comprises metal.

3. The memory array of claim 2 wherein the metal comprises a refractory metal.

4. The memory array of claim 1 wherein the portion of the wordline bypassed by the strapping line comprises a first half of the memory cells coupled to the wordline.

5. A memory array, comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

a number of wordlines coupled to the gate region of at least one memory cell;

a plurality of strapping lines of lower resistance than the wordlines coupled to at least one of the number of wordlines wherein the strapping lines bypass a plurality of portions of a single wordline; and

a plurality of channels connecting the plurality of strapping layers to the wordline.

6. The memory array of claim 5 wherein the plurality of strapping lines comprise metal.

7. The memory array of claim 6 wherein the metal comprises a refractory metal.

8. A memory device, comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

an array of parallel wordlines coupled to the gate region of at least one memory cell, the array of parallel wordlines having a pitch;

a number of strapping devices which bypass portions of the wordlines in the array of parallel wordlines, each strapping device comprising:

a strapping line of lower resistance than the wordlines, wherein the strapping lines are each located a distance from each other that is greater than the pitch; and

at least two channels connecting the strapping line to the wordline.

9. The memory device of claim 8 wherein the strapping line comprises metal.

10. The memory device of claim 9 wherein the metal comprises a refractory metal.

11. The memory device of claim 8 wherein the portions of the wordlines in the array bypassed by the number of strapping devices comprises a plurality of end portions of the wordlines.

12. The memory device of claim 8 wherein the strapping devices are located on alternating wordlines in the array.

13. The memory device of claim 8 wherein the strapping devices are located on adjacent wordlines and staggered along the wordlines such that the portions of the adjacent wordlines that are bypassed are not adjacent to each other.

14. The memory device of claim 8 wherein the strapping devices strap a first half portion of a number of even wordlines in the array and a second half portion of a number of odd wordlines.

15. An integrated circuit comprising:

at least one memory array comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

a number of wordlines coupled to the gate region of at least one memory cell;

at least one strapping line of lower resistance than the wordlines coupled to at least one of the number of wordlines wherein the strapping line bypasses a portion of the wordline;

at least two channels connecting the strapping line to the wordline;

a row decoder;

a column decoder; and

a sense amplifier.

16. The integrated circuit of claim 15 wherein the strapping line comprises metal.

17. The integrated circuit of claim 16 wherein the metal comprises a refractory metal.

18. The integrated circuit of claim 15 wherein the portion of the wordline bypassed by the strapping line comprises a first half of the memory cells coupled to the wordline.

19. An integrated circuit comprising:

at least one memory array comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

an array of parallel wordlines coupled to the gate region of at least one memory cell, the array of parallel wordlines having a pitch;

a number of strapping devices which bypass portions of the wordlines in the array of parallel wordlines, each strapping device comprising:

a strapping line of lower resistance than the wordlines, wherein the strapping lines are each located a distance from each other that is greater than the pitch;

at least two channels connecting the strapping line to the wordline;

a row decoder;

a column decoder; and

a sense amplifier.

20. The integrated circuit of claim 19 wherein the strapping line comprises metal.

21. The integrated circuit of claim 20 wherein the metal comprises a refractory metal.

22. The integrated circuit of claim 19 wherein the portions of the wordlines in the array bypassed by the number of strapping devices comprises a plurality of end portions of the wordlines.

23. The integrated circuit of claim 19 wherein the strapping devices are located on alternating wordlines in the array.

24. The integrated circuit of claim 19 wherein the strapping devices are located on adjacent wordlines and staggered along the wordlines such that the portions of the adjacent wordlines that are bypassed are not adjacent to each other.

25. The integrated circuit of claim 19 wherein the strapping devices strap a first half portion of a number of even wordlines in the array and a second half portion of a number of odd wordlines.

26. An information handling device comprising:

a processing unit;

at least one memory array comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

a number of wordlines coupled to the gate region of at least one memory cell;

at least one strapping line of lower resistance than the wordlines coupled to at least one of the number of wordlines wherein the strapping line bypasses a portion of the wordline;

at least two channels connecting the strapping line to the wordline; and

a system bus connecting the processing unit to the memory array.

27. The information handling device of claim 26 wherein the strapping line comprises metal.

28. The information handling device of claim 27 wherein the metal comprises a refractory metal.

29. The information handling device of claim 26 wherein the portion of the wordline bypassed by the strapping line comprises a first half of the memory cells coupled to the wordline.

30. An information handling device comprising:

a processing unit;

at least one memory array comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

an array of parallel wordlines coupled to the gate region of at least one memory cell, the array of parallel wordlines having a pitch;

a number of strapping devices which bypass portions of the wordlines in the array of parallel wordlines, each strapping device comprising:

a strapping line of lower resistance than the wordlines, wherein the strapping lines are each located a distance from each other that is greater than the pitch;

at least two channels connecting the strapping line to the wordline; and

a system bus connecting the processing unit to the memory array.

31. The information handling device of claim 30 wherein the strapping line comprises metal.

32. The information handling device of claim 31 wherein the metal comprises a refractory metal.

33. The information handling device of claim 30 wherein the portions of the wordlines in the array bypassed by the number of strapping devices comprises a plurality of end portions of the wordlines.

34. The information handling device of claim 30 wherein the strapping devices are located on alternating wordlines in the array.

35. The information handling device of claim 30 wherein the strapping devices are located on adjacent wordlines and staggered along the wordlines such that the portions of the adjacent wordlines that are bypassed are not adjacent to each other.

36. The information handling device of claim 30 wherein the strapping devices strap a first half portion of a number of even wordlines in the array and a second half portion of a number of odd wordlines.

37. A method of reducing a wordline RC time constant comprising:

activating a selected row in a memory array, comprising:

activating a first number of transistors coupled to a first portion of a wordline; and

activating a second number of transistors coupled to a second portion of a wordline, wherein a signal used for activating the second number of transistors bypasses the first portion of the wordline through a

strapping device of lower resistance than the first portion of the wordline;

activating a selected bitline in the memory array associated with a selected memory cell;

discharging the selected memory cell through a selected transistor, the selected transistor being activated by both the selected row and the selected bitline; and

sensing the presence or absence of a charge from the selected memory cell through the use of a sense amplifier.

38. The method of reducing a wordline RC time constant of claim 37, wherein activating a second number of transistors coupled to a second portion of a wordline comprises:

sending a signal through a first channel to a metal strapping line;

sending the signal through the metal strapping line; and

sending the signal through a second channel to the second portion of the wordline.

39. The method of reducing a wordline RC time constant of claim 38, wherein sending the signal through the metal strapping line comprises sending the signal through a refractory metal strapping line.

40. The method of reducing a wordline RC time constant of claim 37, wherein activating a first number of transistors coupled to a first portion of a wordline comprises activating a first number of transistors coupled to a first half of the wordline.

41. The method of reducing a wordline RC time constant of claim 37, wherein activating a selected row in a memory array comprises bypassing multiple portions of the wordline using multiple strapping devices of lower resistance than the wordline.

42. A method of reducing a wordline RC time constant in a memory bank comprising:

activating a plurality of selected coupled wordlines in a plurality of memory arrays, comprising:

activating a first wordline in a first memory array; and

activating a second wordline in a second memory array, wherein a signal used for activating the second wordline bypasses the first wordline through a strapping device of lower resistance than the first wordline;

activating a selected bitline in one of the plurality of memory arrays associated with a selected memory cell;

discharging the selected memory cell through a selected transistor, the selected transistor being activated by both the plurality of selected coupled wordlines and the selected bitline; and

sensing the presence or absence of a charge from the selected memory cell through the use of a sense amplifier.

43. The method of reducing a wordline RC time constant of claim 37, wherein activating a second wordline in a second memory array comprises:

sending a signal through a first channel to a metal strapping line;

sending the signal through the metal strapping line; and

sending the signal through a second channel to the second wordline.

44. The method of reducing a wordline RC time constant of claim 43, wherein sending the signal through the metal strapping line comprises sending the signal through a refractory metal strapping line.

45. A method of forming a memory device comprising:

forming a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

coupling a number of source lines to the first source/drain region of at least one memory cell;

coupling a number of bit lines to the second source/drain region of at least one memory cell;

attaching a number of wordlines to the gate region of at least one memory cell;

attaching at least one strapping line of lower resistance than the wordlines to at least one of the number of wordlines wherein the strapping line bypasses a portion of the wordline; and

connecting the strapping line to the wordline by forming at least two channels from the strapping line to the wordline.

46. The method of forming a memory device of claim 45, wherein attaching at least one strapping line of lower resistance than the wordlines to at least one of the number of wordlines comprises attaching at least one metal strapping line.

47. The method of forming a memory device of claim 46, wherein attaching at least one metal strapping line comprises attaching at least one refractory metal strapping line.

48. The method of forming a memory device of claim 45, wherein attaching at least one strapping line of lower resistance than the wordlines to at least one of the number of wordlines comprises attaching multiple strapping lines to bypass multiple portions of a single wordline.

49. A method of forming a memory device comprising:

forming a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

coupling a number of source lines coupled to the first source/drain region of at least one memory cell;

coupling a number of bit lines coupled to the second source/drain region of at least one memory cell;

attaching an array of parallel wordlines to the gate region of at least one memory cell, the array of parallel wordlines having a pitch;

attaching a number of strapping lines of lower resistance than the wordlines which bypass portions of the wordlines in the array of parallel wordlines, wherein the

strapping lines are each located a distance from each other that is greater than the pitch; and

connecting the strapping lines to the wordlines by forming at least two channels from each strapping line to the wordline.

50. The method of forming a memory device of claim 49, wherein attaching a number of strapping lines comprises attaching a number of metal strapping lines.

51. The method of forming a memory device of claim 50, wherein attaching a number of metal strapping lines comprises attaching a number of refractory metal strapping lines.

52. The method of forming a memory device of claim 49, wherein attaching a number of strapping lines comprises attaching the strapping lines on alternating wordlines in the array.

53. The method of forming a memory device of claim 49, wherein attaching the strapping lines comprises attaching the strapping lines on adjacent wordlines and staggering the strapping lines along the wordlines such that the portions of the adjacent wordlines that are bypassed are not adjacent to each other.

54. The method of forming a memory device of claim 49, wherein attaching a number of strapping lines comprises attaching the strapping lines on a first half portion of a number of even wordlines in the array and attaching the strapping lines on a second half portion of a number of odd wordlines.